What is claimed is:

1. A method for forming a trench capacitor, the method comprising:

forming a trench in a semiconductor substrate;

depositing a conformal layer of semiconductor material in the trench;

roughening the surface of the conformal layer of semiconductor material;

forming an insulator layer outwardly from the roughened, conformal layer of semiconductor material; and

forming a polycrystalline semiconductor plate outwardly from the insulator layer in the trench.

2. The method of claim 1, wherein depositing a conformal layer of semiconductor material comprises depositing a layer of amorphous silicon and heating the amorphous silicon to form a polysilicon layer of the same conductivity type as the adjacent semiconductor substrate.

3. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with a phosphoric acid etch.

4. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with an anodic etch.

5. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with an anodic etch including illuminating the conformal layer of semiconductor material during the anodic etch.

6. The method of claim 1, wherein forming an insulator layer comprises growing an oxide layer outwardly from the roughened, conformal layer of semiconductor material.

7. A method for forming a memory cell with a trench capacitor, comprising:

forming a transistor including first and second source/drain regions, a body region and a gate in a layer of semiconductor material on a substrate;

forming a trench in the layer of semiconductor material;

depositing a conformal layer of semiconductor material in the trench;

roughening the surface of the conformal layer of semiconductor material;

forming an insulator layer outwardly from the roughened, conformal layer of semiconductor material;

forming a polycrystalline semiconductor plate outwardly from the insulator layer in the trench such that the polycrystalline semiconductor plate forms one of the plates of the trench capacitor; and

coupling the trench capacitor to one of the source/drain regions of the transistor.

8. The method of claim 7, wherein forming a transistor comprises forming a transistor with first and second source drain regions that are vertically aligned with the body region.

9. The method of claim 8, wherein coupling the trench capacitor to the first source/drain region comprises forming the trench for the trench capacitor adjacent to the first source/drain region.

10. The method of claim 7, wherein forming a transistor comprises forming a lateral transistor.

11. The method of claim 10, wherein coupling the trench capacitor to the first source/drain region comprises forming a strap from the polycrystalline semiconductor plate to the first source/drain region.

12. The method of claim 7, wherein depositing a conformal layer of semiconductor material comprises depositing a layer of amorphous silicon and heating the amorphous silicon to form a poly-silicon layer of the same conductivity type as the adjacent semiconductor substrate.

13. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with phosphoric acid.

14. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises performing an anodic etch of a surface of the semiconductor material.

15. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises performing an anodic etch of a surface of the semiconductor material while illuminating the semiconductor material.

16. The method of claim 7, wherein forming an insulator layer comprises growing an oxide layer outwardly from the roughened, conformal layer of semiconductor material.

17. A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region;

a trench capacitor formed in a trench and coupled to the first source/drain region; and

wherein the trench capacitor includes a polycrystalline semiconductor plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polycrystalline semiconductor material on the surface of the substrate, and an insulator layer that separates the polycrystalline semiconductor plate from the roughened surface of the substrate.

18. The memory cell of claim 17, wherein the polycrystalline semiconductor plate comprises polysilicon.

19. The memory cell of claim 17, wherein the second plate comprises a heavily doped p-type silicon substrate.

20. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a surface in the trench that is roughened by an anodic etch.

21. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a surface in the trench that is roughened by a phosphoric etch.

22. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the first source/drain region is roughened by etching a polycrystalline semiconductor material on a surface of the first source/drain region; and

a trench capacitor with a plate that is formed in a trench that surrounds the roughened surface of the first source/drain region of the transistor.

23. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with phosphoric acid.

24. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with an anodic etch.

25. The memory cell of claim 22, wherein the polycrystalline semiconductor plate comprises polysilicon.

26. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon and a second plate of the trench capacitor is disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. The memory device of claim 26, wherein the first plate comprises a single crystalline silicon source/drain region of a vertical transistor with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with phosphoric acid.

28. The memory device of claim 26, wherein the first plate comprises a single crystalline silicon source/drain region of a vertical transistor with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with an anodic etch.

29. The memory device of claim 26, wherein the polycrystalline semiconductor plate comprises polysilicon.

30. The memory device of claim 29, wherein the access transistor comprises a lateral transistor that is coupled to the second plate of the trench capacitor.